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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,673	07/11/2005	Matthias Muth	DE02 0143 US	1887

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/517,673	MUTH, MATTHIAS	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 5/16/2007.

2. Claims 1-17 have been cancelled and claims 18-21 have been added. Thus, claims 18-21 are pending.

Information Disclosure Statement

The information disclosure statement filed on 12/07/2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. The document ID 4226704 mentioned on IDS but is not in the record. Therefore, the IDS has been placed in the application file, but the information referred to therein has not been considered.

Claim Objections

Claim 18 is objected to because of the following informalities:

Claim 18 recites the voltage controllers in lines 17-19, which lack antecedent basis. For the rest of the action it is assumed that "first and second voltage regulators" were intended, which were recited in lines 10 and 14. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Heinrich et al (US Patent 6470393).

For claim 21, Heinrich et al teach the following limitations:

A method of conserving operating power (lines 37-42 of column 2) **in a bus-oriented system** (Fig 1) **with many applications processors** (Fig 1 and Fig 2) **comprising:**

- **providing constant power from a primary power supply to a plurality of bus transceivers** (lines 10-12 of column 1 mentions that each node is capable of constituting transmitter/receiver. Thus, part of "IF" in Fig 2 responsible for transmitting/receiving is the transceiver) **each connected to a respective node on a bus** (Vbat on line 15 provides power to the nodes);
- **monitoring said bus for data activity** (lines 54-67 of column 6 mention that DF is fed with Rx as signal to be differentiated. Therefore, data activity is monitored on the bus) **and if such activity is detected then, enabling a higher power mode of operation for said bus transceivers** (high power mode is only enabled if detected data matches with pre-selected data; lines 60-65 of column

2) **and powering up a data decoder** (lines 38-60 of column 5 mention that contents of ASR are compared with contents of address filter AF. Thus, the contents of ASR are decoded to know whether they match with contents of AF. Thus, data decoder is powered when data activity is detected);

- **decoding said data activity with said data decoder** (lines 38-60 of column 5 mention that contents of ASR are compared with contents of address filter AF. Thus, the contents of ASR are decoded to know whether they match with contents of AF) **and providing a gate signal if a particular message storage is recognized** (lines 55-60 of column 5 mentions that output of AND depends on the conformity of comparison. Lines 33-38 of column 6 mention that logic output of AND gate signals that received address is the intended address. Thus, MR provides appropriate output when addresses match);
- **powering up a corresponding applications processor as long as its associated gate signal is being received** (lines 60-65 of column 2 mention that activating address effects in activation of voltage controller and microcontroller);
- **wherein, each particular applications processor is powered up for so long as there is data activity and particular messages on said bus are recognized** (microcontrollers are powered up only when there is an activating address as mentioned in lines 60-65 of column 2), **wherein overall operating power taken from the primary power supply is conserved by operating said data decoder in a medium power mode when data activity is detected** (node

can be maintained in low power mode when no data is transmitted via the bus line and interfaces are set to active state when activating demand is transmitted via the bus. Therefore, interfaces are in active state when there is an activating demand. That is the medium power mode), **and then only operating each applications processor when they have been addressed and selected to operate determined by the corresponding data decoder** (lines 60-65 of column 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heinrich et al (US Patent 6470393), in view of Hanf et al (US Patent 5892893).

For claim 18, Heinrich et al teach the following limitations:

A bus interface and power control system (Fig 1), **comprising:**

- **a connection for a primary power supply** (15);
- **a transceiver** (lines 10-12 of column 1 mentions that each node is capable of constituting transmitter/receiver. Thus, part of "IF" in Fig 2 responsible for

transmitting/receiving is the transceiver) **providing a data interface** (DF) **to a single node** (DK) **on a data communication bus** (13) **and able to provide a bus activity signal** (S/R on Fig 4) **when data activity is monitored on the data communication bus** (lines 54-67 of column 6 mention that DF is fed with Rx as signal to be differentiated. Therefore, data activity is monitored on the bus) **during a low power mode supported by the primary power supply** (lines 50-60 of column 2 mentions that interface can be kept low power mode when no data transmitted over the bus line. When an activating demand is placed, interfaces are set to active state. Thus, data can be monitored during low power mode to determine whether activating demand is transmitted via the bus. If data activity is present on the bus during low power mode, S/R signal is generated to perform the address filtering);

- **a protocol controller** ("Address filter" part shown in Fig 3 comprising ASR, AF, MR, AND) **for decoding data messages passed through the transceiver from said data communication bus** (lines 38-60 of column 5 mention that contents of ASR are compared with contents of address filter AF. Thus, the contents of ASR are decoded to know whether they match with contents of AF), **and for providing a gate signal when a decoded message matches a particular pattern in storage** (lines 55-60 of column 5 mentions that output of AND depends on the conformity of comparison. Lines 33-38 of column 6 mention that logic output of AND gate signals that received address is the intended address. Thus, MR provides appropriate output when addresses match);

- **a second voltage regulator** (UR in Fig 2) **for supplying operating power in a high power mode to an applications processor** (MC) **when said gate signal is received** (lines 60-65 of column 2 mention that activating address effects in activation of voltage controller and microcontroller);
- **wherein, second voltage controller is off during said low power mode** (voltage controller only activates when activating address is intended for that node presents as mentioned in lines 60-65 of column 2)

Heinrich does not explicitly mention the following limitations:

- first controller is off during low power mode, a first voltage regulator for supplying additional power to the transceiver and for supplying operating power to the protocol controller, both in a medium power mode engaged when said bus activity signal is received;
- the first voltage controller is on during said medium power mode, and both the first and second voltage controllers are on during said high power mode;
- and wherein, said low power mode of operation is returned to automatically

For the first limitation, "a first voltage regulator for supplying additional power to the transceiver and for supplying operating power to the protocol controller, both in a medium power mode engaged when said bus activity signal is received", Heinrich teaches that node can be maintained in low power mode when no data is transmitted via the bus line and interfaces are set to active state when activating demand is transmitted via the bus. Therefore, interfaces are in active state when there is an

activating demand. That is the medium power mode for the protocol controller. Such mode requires additional power as needed to set itself into active state from the low power state. Fig 2 shows that IF takes power from line 15. Thus, when activating demand is in bus, protocol controller (i.e., part of interface) gets power from 15 to set into active state. Therefore, IF must comprise a first voltage controller that would determine when to supply the additional voltage for address filter (or, protocol controller). For the limitations "the first voltage controller is on during said medium power mode, and both the first and second voltage controllers are on during said high power mode", the first voltage regulator has to be turned on during medium power mode (or, the active state of interface) and the two regulators have to be turned on during high power mode for proper working. Therefore, these limitations are within the spirit of Heinrich.

For the limitations, "wherein, said low power mode of operation is returned to automatically", Heinrich et al teach return of low power mode (lines 50-55 of column 2 mention that interfaces can be held in low power mode). However, Heinrich does not mention that low power mode is returned automatically.

Examiner takes an official notice that return of low power mode due to inactivity is well known in the art. One ordinary skill would be motivated to return low power mode to conserve the energy.

Heinrich does not mention turning off the first voltage controller during low power mode. Hanf et al mention turning off the first voltage controller during low power mode (lines 44-46 of column 15).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Heinrich and Hanf. One ordinary skill would be motivated to turn off the voltage controller as it conserves more power.

For claim 19, lines 60-65 of column 2 of Heinrich mention that voltage controller and microcontroller are activated. Lines 25-30 of column 5 mention that MC is fed with UR. Therefore, the initial providing of voltage to MC can be though as reset after activation of UR and MC.

For claim 20, Fig 1 and Fig 2 of Heinrich show the plural addressable nodes on bus with application processors MC such that pre-selected messages can power up (lines 60-65 of column 2) and power down (absence of messages can power down the nodes) processors MC and conserve the power taken from primary power supply.

Response to Arguments

Applicant's arguments filed on 5/16/2007 have been fully considered but they are not persuasive.

Applicant argues that Heinrich involves only one stage of power control and it requires addressing to engage the power control.

Examiner agrees that Heinrich requires addressing to engage power control. However, such feature of Heinrich is not prohibited in the claimed invention. Thus, these arguments are irrelevant for the claimed invention.

Examiner disagrees that Heinrich involves only one stage of control. Lines 50-55 of column 2 of Heinrich teaches that node can be maintained in low power mode when no data is transmitted via the bus line and lines 48-60 of column 2 mention that interfaces are set to active state when activating demand is transmitted via the bus. Therefore, interfaces are in active state when there is an activating demand. That is the medium power mode for the protocol controller. Such mode requires additional power as needed to set itself into active state from the low power state. Lines 60-65 of Heinrich disclose the high power mode where microcontroller and voltage controller are activated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

THUAN N. DU
PRIMARY EXAMINER